## REMARKS/ARGUMENTS

### *Brief Summary of Status*

Claims 1-184 are pending in the application.

Claims 129-133 are allowed.

Claims 1-128, and 134-184 are rejected.

### *Claim Rejections - 35 U.S.C. § 102*

4. In the office action, the Examiner states:

"Claims 1-27, 35-37, 39-57, 60, 63-69, 72, 76-79, 113-117, 119-124,126-127, 134-160, 163, 168-170, 184 are rejected under 35 U.S.C. 102(b) as being anticipated by Womack et al (5,982,819)." (hereinafter referred to as "Womack") (office action, Part of Paper No./Mail Date 20061002, p. 2).

5. In the office action, the Examiner states:

"Claims 1-37, 42-69, 72-75, 79, 80-103, 105-112, 113-126-128, 134-170, 172-184 are rejected under 35 U.S.C. 102(b) as being anticipated by Stewart (5,671,253)." (hereinafter referred to as "Stewart") (office action, Part of Paper No./Mail Date 20061002, p. 3).

6. In the office action, the Examiner states:

"Claims 1, 38, 42, 70-71, 80, 104, 113, 128, 134, 171 are rejected under 35 U.S.C. 102(e) as being anticipated by Phanse et al. (6,795,494)." (hereinafter referred to as "Phanse") (office action, Part of Paper No./Mail Date 20061002, p. 4).

### *Allowable Subject Matter*

7. In the office action, the Examiner states:

"Claims 129-133 are allowed." (office action, Part of Paper No./Mail Date 20061002, p. 4).

***Claim Rejections - 35 U.S.C. § 102***

4. In the office action, the Examiner states:

"Claims 1-27, 35-37, 39-57, 60, 63-69, 72, 76-79, 113-117, 119-124,126-127, 134-160, 163, 168-170, 184 are rejected under 35 U.S.C. 102(b) as being anticipated by Womack et al (5,982,819)." (hereinafter referred to as "Womack") (office action, Part of Paper No./Mail Date 20061002, p. 2).

The Applicant respectfully traverses.

The Applicant respectfully points out that, in order to support a proper rejection under 35 U.S.C. §102, a singular reference must teach and disclose each and every limitation of the subject matter as claimed by the Applicant. If the singular reference fails to teach and disclose each and every limitation of the subject matter as claimed by the Applicant, the rejections under 35 U.S.C. § 102 should be withdrawn.

The Applicant respectfully points out that Womack fails to teach and disclose each and every limitation of the subject matter as claimed by the Applicant.

The Examiner also asserts:

"Womack discloses a digital signals processing comprising: a receiver that includes an analog to digital converter ((409); and digital signal processor (401), the digital signal processor is operable coupled to an output of the analog to digital converter. The analog to digital converter samples the modulated serial data to generate digital samples data; and the digital signal processor determines compensation operation to be performed by the receiver on the digital samples. The digital signal processing interfaces two devices communicatively coupled via a cable. The receiver further comprises a plurality of programmable gain amplifiers (425,427) coupled to the analog to digital converter; an automatic gain control (403); a memory (410,412). The digital signal processing determines at least one of an error in gain, an error in phase, and an error in offset. The receiver further comprises an analog circuitry (420,422,426) located before and communicatively coupled to the analog to digital converter. The receiver further comprises a plurality of analog to digital converters. The receiver further comprises a decoder(418,114) that operable to decode the digital samples. The digital processing employs parallel processing compensation techniques. The digital signal processing further comprises a transmitter and receiver. The receiver further comprises a timing

recovery (407).(see fig.4 col.4, line 1 to col.5, line 67)." (office action, Part of Paper No./Mail Date 20061002, p. 2-3, emphasis added)

The Applicant respectfully believes that Womack fails to teach and disclose subject matter that includes a digital signal processor that adaptively determines compensation operations to be performed by the receiver on the digital samples of the modulated serial data so that the digital samples of the modulated serial data may be properly characterized to extract digital data contained therein. The Applicant respectfully believes that Phanse likewise fails to teach and disclose each and every limitation of the subject matter as claimed by the Applicant in the Applicant's independent claim 1 and the Applicant's other independent claims.

The Applicant also respectfully believes that Womack explicitly teaches and discloses that the means performed to assist in the demodulation and decoding of base band data therein is performed using pre-stored means or using programmable means; the Applicant respectfully believes that the means employed by Womack is not adaptively determined.

Womack teaches and discloses:

"Referring to FIG. 4, a messaging receiver (400) is shown. It relies on a general, programmable signal processing architecture and an intelligent, fast-reacting operating system to accomplish its goals. It must be able to receive over multiple forward and reverse channels and handle virtually any modulation type. To do this, the analog IF signal must be sampled at a high data rate and fed to programmable down converters that recover the base band data. At base band, a digital signal processor (DSP) is ready with the necessary algorithms pre-stored in resident memory to demodulate and decode the data. The number of messaging protocols or modulation formats the receiver can demodulate or recover is limited by the computational power of its DSP based processor and the size of its memory. In any event, the recovered message is routed back to the controller through the network processor or network interface." (Womack, col. 4, lines 1-16, emphasis added)

Clearly, the programmability functionality of the "down converters" is made to "recover the base band data".

Womack does not teach and disclose that any parameters (e.g., the programmability of these "down converters") are adaptively determined performed by any DSP (i.e., not by the "processor 401" of Womack that the Examiner identifies as digital signal processor (401)).

Womack teaches and discloses a "messaging receiver (400) and corresponding system (100b) and method adaptable to a plurality of modulation formats". (Womack, ABSTRACT, lines 1-3, emphasis added)

The functionality described in Womack appears to be concerned with a means by which a system can switch between multiple "modulation formats", and it is in fact a "controller 403" of Womack helps effectuate that goal. It is not the "processor 401" of Womack that effectuates that goal.

Womack teaches and discloses:

"The controller (403) is responsive to the modulation identifier or format and is utilized for deploying the flexible resources (404) and radio frequency circuits in accordance therewith. With the flexible resources deployed in accordance with the modulation identifier or format, the receiver may receive further signals having corresponding modulation formats." (Womack, col. 4, lines 1-16, emphasis added)

As can be seen also when considering FIG. 4 of Womack, there are a number of control type signals that are fed back to the analog portion (i.e., to elements situated before the A/Ds 409 and the "digital converters 411") of the "messaging receiver (400)" of FIG. 4 of Womack. The Applicant respectfully believes that Womack teaches and discloses, at a very minimum, an approach such that programmability of the system therein involves governing by the "controller (403)" in at least the "analog" domain; the "controller (403)" must control the "flexible resources (404)" within the analog domain and clearly is not adaptive determination of compensation operations to be performed by the receiver on the digital samples of the modulated serial data. Womack teaches and discloses the governing of the governing by the "controller (403)" of the "flexible resources (404)" within the analog domain.

The Applicant respectfully believes that the operations in accordance with Womack necessarily require this analog domain operation, as governed by the "flexible

resources (404)", and the Applicant respectfully believes that this is a departure from the subject matter as claimed by the Applicant.

Moreover, as cited above, Womack teaches and discloses: "[a]t base band, a digital signal processor (DSP) is ready with the necessary algorithms pre-stored in resident memory to demodulate and decode the data".

As can be seen, the "algorithms" employed by the "DSP" of Womack are not "adaptively determined"; they are "pre-stored in resident memory". The Applicant respectfully believes that this is in contradistinction to the subject matter as claimed by the Applicant.

The use of "algorithms pre-stored in resident memory to demodulate and decode the data" is in contradistinction to the subject matter as claimed by the Applicant that includes at least a digital signal processor that adaptively determines compensation operations to be performed by the receiver on the digital samples of the modulated serial data so that the digital samples of the modulated serial data may be properly characterized to extract digital data contained therein. In Womack, the DSP therein does not perform any "adaptive determination" to identify any algorithms "to demodulate and decode the data"; in contradistinction, Womack employs "algorithms pre-stored in resident memory to demodulate and decode the data". The Applicant respectfully believes that the operations as performed by the DSP of Womack do not involve adaptive determination (i.e., the algorithms are pre-stored in Womack).

Moreover, Womack explicitly teaches and discloses that, at the time of the filing of the U.S. patent 5,982,819 that DSPs were incapable of performing such adaptively determined digital-based compensation.

Womack teaches and discloses:

"At present, given the performance limitations of DSPs, radio frequency signals at higher frequencies are less likely to be implemented in DSPs." (Womack, col. 5, lines 14-15, emphasis added)

Womack makes an attempt to predict the future (as cited below), but there is absolutely no enabling description in Womack in which DSPs are capable of performing such digital-based compensation.

Womack teaches and discloses:

"As advances are made in DSP technology it is likely that more and more of the functionality of the radio frequency circuits will be implemented in the processor (401)." (Womack, col. 5, lines 10-12, emphasis added)

The Applicant respectfully believes that such a future-reaching guess, as may by Womack, that "it is likely" that something *may happen* in the future is not enabling written description and does not teach and disclose subject matter that anticipates the subject matter as claimed by the Applicant.

As cited above, Womack explicitly teaches and discloses that "[a]t present, given the performance limitations of DSPs, radio frequency signals at higher frequencies are less likely to be implemented in DSPs"; and, when Womack describes "[a]t present", this refers to the time of filing of the U.S. patent 5,982,819, and the Applicant respectfully believes that Womack's characterization teaches and discloses that the use of DSPs to perform any adaptively determined digital-based compensation is beyond the capability of the technology of that time.

Therefore, in light of at least these comments made above, the Applicant respectfully believes that Womack fails to teach and disclose each and every limitation of the subject matter as claimed by the Applicant in each of independent claims indicated above that the Examiner rejects as being anticipated by Womack.

The Applicant also respectfully believes that the dependent claims indicated above that the Examiner rejects as being anticipated by Womack, being further limitations of the subject matter as claimed in allowable independent claims are also allowable.

As such, in light of at least these comments made above, the Applicant respectfully requests that the Examiner withdraw the rejection of claims 1-27, 35-37, 39-57, 60, 63-69, 72, 76-79, 113-117, 119-124,126-127, 134-160, 163, 168-170, 184 under 35 U.S.C. § 102(b) as being anticipated by Womack.

5. In the office action, the Examiner states:

"Claims 1-37, 42-69, 72-75, 79, 80-103, 105-112, 113-126-128, 134-170, 172-184 are rejected under 35 U.S.C. 102(b) as being anticipated by Stewart (5,671,253)."

(hereinafter referred to as "Stewart") (office action, Part of Paper No./Mail Date 20061002, p. 3).

The Applicant respectfully traverses.

The Applicant respectfully points out that, in order to support a proper rejection under 35 U.S.C. §102, a singular reference must teach and disclose each and every limitation of the subject matter as claimed by the Applicant. If the singular reference fails to teach and disclose each and every limitation of the subject matter as claimed by the Applicant, the rejections under 35 U.S.C. § 102 should be withdrawn.

The Applicant respectfully points out that Stewart fails to teach and disclose each and every limitation of the subject matter as claimed by the Applicant.

The Examiner also asserts:

"Stewart discloses a digital signal-processing receiver comprising a receiver including an analog to digital converter (2.10) coupled to a digital signal processor (10). The digital coveter samples the modulated data to generate digital samples and the digital signal processor determines compensation operation to be performed by the receiver. The signal processing further comprises programmable gain amplifier (2050; an automatic gain control circuitry ((270). The digital signal processing is implemented in data communication application. .the digital signal processing determines at least one of an error in gain, an error in phase and an error in offset. The signal processing further comprises a filter (235) and an equalizer(220) and further comprises a Viterbi decoder that is operable to decode the digital samples of the modulated signal. (see figs. 1-2, and 5)." (office action, Part of Paper No./Mail Date 20061002, p. 3-4, emphasis added)

The Examiner refers to reference numeral "10" of Stewart as a "digital signal processor (10)".

Stewart teaches and discloses:

"In FIG. 1, a carrier modulated with video data is received by an antenna 15, processed and digitized by network 20. The resultant digital output signal is demodulated by demodulator 10 and decoded by decoder 12. The output from decoder 12 is further processed to provide decompressed output video data suitable for display by a display device. Both demodulator 10 and decoder 12 are adaptive demodulation and decoding networks incorporating different types of demodulation and decoding functions which are

selected by microcontroller 105 via interface 100. Both demodulator 10 and decoder 12 are configured by a Control signal from microcontroller interface 100. The status of the Control signal provided by interface 100 is determined by signals provided by microcontroller 105 to interface 100." (Stewart, col. 5, lines 10-12, emphasis added)

It is clear that the reference numeral "10" of Stewart actually corresponds to a "demodulator 10".

The Applicant respectfully points out that this "demodulator 10" of Stewart does not perform any adaptive determination of compensation operations to be performed by the receiver on the digital samples of the modulated serial data so that the digital samples of the modulated serial data may be properly characterized to extract digital data contained therein.

The "demodulator 10" of Stewart is essentially a device whose operation is governed by the "microcontroller 105". FIG. 1, FIG. 2, and FIG. 5 of Stewart all show and/or correspond to operation of a "microcontroller 105" that provides control to certain components of the corresponding system.

As Stewart describes, any reconfiguration of the "demodulator 10" of Stewart, that the Examiner refers to as a "digital signal processor (10)" is performed by the "microcontroller 105"; the "demodulator 10" itself does not perform any adaptive determination of compensation operations to be performed by the receiver on the digital samples of the modulated serial data so that the digital samples of the modulated serial data may be properly characterized to extract digital data contained therein.

The "demodulator 10" of Stewart is in fact configurable (even re-configurable), but the "demodulator 10" itself does not perform any adaptive determination of compensation operations including any adaptive determination of compensation operations of operations that it performs. According to Stewart, these are determined by the "microcontroller 105".

"Configurable demodulator 10 provides the functions required for demodulating each of the DSS and DVB signal formats. The primary functions of demodulator 10 are recovery and tracking of the carrier frequency, recovery of the transmitted data clock frequency, and recovery of the video data itself. In addition, the demodulator includes an AGC network (FIG. 5) to appropriately scale analog input data prior to analog to digital

conversion in unit 20. The demodulator functions are implemented by units 25, 30, 35, 40 and 45. Timing recovery, carrier recovery, slicer and differential decoder operations are individually known and generally described, for example, in the reference text Digital Communication, Lee and Messerschmidt (Kluwer Academic Press, Boston, Mass., USA, 1988)." (Stewart, col. 3, lines 6-18, emphasis added)

Another portion of Stewart explicitly teaches and discloses that it is the "microcontroller 105" that performs the re-configuration of the "demodulator 10". The "demodulator 10" of Stewart, that the Examiner refers to as a "digital signal processor (10)" actually performs no re-configuration or determination of any parameters employed for any re-configuration. In contradistinction, the "demodulator 10" is governed by, and re-configured by the "microcontroller 105".

Stewart teaches and discloses:

"Signal quality detector 275 estimates the signal to noise ratio (SNR) of the input signal to demodulator 10 using the AGC error signal provided by unit 270. Unit 270 first forms the absolute value of the AGC error signal. Then unit 270 applies decision thresholds to the result to determine whether the AGC error lies within a programmed range of values. This provides a determination of the magnitude of the AGC error value which corresponds to an estimate of SNR value. This SNR estimate is provided to microcontroller 105 via interface 100 in FIG. 1. Microcontroller 105 is programmed to determine whether the SNR value lies outside a predetermined range. If the SNR value is outside the predetermined range, microcontroller 105 may re-configure the system including all the configurable elements of demodulator 10, equalizer 220 and decoder 12 for a different input signal format. In this way, microcontroller 105 may iteratively re-configure demodulator 10 and decoder 12 functions by using the Control signal via interface 100 to appropriately demodulate and decode the applied input signal format. This configuration function may be programmed to be performed as part of an initialization procedure or in response to an input signal to the microcontroller from an operator accessible switch, for example." (Stewart, col. 6, lines 35-57, emphasis added)

As can be seen, it is (1) when the "AGC error value which corresponds to an estimate of SNR value" is "outside the predetermined range" which triggers the (2) (microcontroller 105) possibly to perform the (3) re-configuration of the system.

Clearly, the "demodulator 10" of Stewart, which the Examiner refers to as a "digital signal processor (10)", does neither performs any adaptive determination of any re-configuration operations nor re-configures itself. Again, the "demodulator 10" is governed by, and re-configured by the "microcontroller 105".

Therefore, in light of at least these comments made above, the Applicant respectfully believes that Stewart fails to teach and disclose each and every limitation of the subject matter as claimed by the Applicant in each of independent claims indicated above that the Examiner rejects as being anticipated by Stewart.

The Applicant also respectfully believes that the dependent claims indicated above that the Examiner rejects as being anticipated by Stewart, being further limitations of the subject matter as claimed in allowable independent claims are also allowable.

As such, in light of at least these comments made above, the Applicant respectfully requests that the Examiner withdraw the rejection of claims 1-37, 42-69, 72-75, 79, 80-103, 105-112, 113-126-128, 134-170, 172-184 under 35 U.S.C. § 102(b) as being anticipated by Stewart.

6. In the office action, the Examiner states:

"Claims 1, 38, 42, 70-71, 80, 104, 113, 128, 134, 171 are rejected under 35 U.S.C. 102(e) as being anticipated by Phanse et al. (6,795,494)." (hereinafter referred to as "Phanse") (office action, Part of Paper No./Mail Date 20061002, p. 4).

The Applicant respectfully traverses.

The Applicant respectfully points out that, in order to support a proper rejection under 35 U.S.C. §102, a singular reference must teach and disclose each and every limitation of the subject matter as claimed by the Applicant. If the singular reference fails to teach and disclose each and every limitation of the subject matter as claimed by the Applicant, the rejections under 35 U.S.C. § 102 should be withdrawn.

The Applicant respectfully points out that Phanse fails to teach and disclose each and every limitation of the subject matter as claimed by the Applicant.

The Examiner also asserts:

"Consider claim 1,38,42,70-71,80,104,113,128,134,171 as claimed . Phanse discloses a digital signal processing comprising a receiver including an analog to digital

converter for sampling the data coupled to a digital signal processor for determining a compensation operation and a crosstalk canceller.(see fig. 1 abstract)." (office action, Part of Paper No./Mail Date 20061002, p. 4, emphasis added)

The Applicant respectfully points out that FIG. 1 of Phanse does not include any digital signal processor whatsoever.

The first mention in Phanse of anything like a digital signal processor is with reference to FIG. 7 and is cited as follows:

Phanse teaches and discloses:

"The digital back-end of full-duplex transceiver 700 comprises digital FIR filter 150, digital signal processor (DSP) echo canceller and near-end crosstalk (NEXT) canceller 710, DSP automatic gain control (AGC) circuit 720, DSP base line wander (BLW) circuit 730, DSP adaptive controller 740, and slicer 155. Digital FIR filter 150 and slicer 155 are the same as in full-duplex transceiver 100. However, digital FIR controller 180 has been replaced by DSP adaptive controller 740, which not only generates coefficients for digital FIR filter 150, but also controls the operations of DSP echo canceller and NEXT canceller 710, DSP AGC circuit 720, and DSP BLW circuit 730." (Phanse, col. 11, lines 27-38, emphasis added)

In performing the "digital signal processing" capabilities within FIG. 7 of Phanse, Phanse employs at least 4 separate devices:

1. digital signal processor (DSP) echo canceller and near-end crosstalk (NEXT) canceller 710;
2. DSP automatic gain control (AGC) circuit 720;
3. DSP base line wander (BLW) circuit 730; and
4. DSP adaptive controller 740.

As the Applicant describes in more detail below with respect to Phanse, FIG. 7 operates using digital domain compensation in conjunction with analog domain based compensation.

The Applicant in unable to find anywhere in FIG. 1 of Phanse or the associated description thereof that both of the analog and digital means of equalization are not needed for proper operation. In contradistinction, Phanse seems only to indicate that the

BOTH analog and digital compensation are performed, and only when both are performed, does the compensation for the system of FIG. 1 actually converge.

More specifically, the Applicant respectfully asserts that Phanse does not teach and disclose a digital signal processed based serializer/de-serializer that adaptively determines compensation to be performed by the receiver on the digital samples of the modulated serial data so that the digital samples of the modulated serial data may be properly characterized to extract digital data contained therein.

In contradistinction, Phanse teaches and discloses a "mixed mode equalization" approach in many locations such that "analog equalization" as well as "digital equalization" both need to be performed for proper operation. In fact, the Applicant respectfully asserts that the teaching and disclosure of Phanse is such that the only means by which the "digital equalization" can operate effectively is with the assistance of the "analog equalization". Similarly, the Applicant respectfully asserts that the teaching and disclosure of Phanse is such that the only means by which the "analog equalization" can operate effectively is with the assistance of the "digital equalization". Moreover, it appears that the majority of compensation operations are performed in the analog domain, and the digital domain just performs any remaining, fine-tuning compensation when compared to the analog domain compensation.

The Applicant provides some examples from Phanse that describes this inherent dual analog means in combination with digital means of performing compensation.

"The present invention implements a mixed mode equalization in which analog equalization is performed by adaptive equalization filter 140 and digital equalization is performed by digital FIR filter 150. The mixed mode equalization occurs in alternating digital and analog stages until convergence (or a time out) occurs." (Phanse, col. 10, lines 5-10, emphasis added)

"FIG. 6 depicts flow diagram 600, which illustrates the mixed mode equalization operation of exemplary full-duplex transceiver 100 according to one embodiment of the present invention. The mixed mode adaptive equalization filter provides signal equalization in the form of a high frequency boost that offsets cable loss. The amount of high frequency boost of the equalizer adapts to the length of the attached cable. Adaptive equalization filter (AEF) 140 is controlled (adapted) in conjunction with digital FIR filter

160. The mixed mode equalization scheme provides some analog and some digital equalization to compensate for the overall attenuation of the channel. AEF 140 is incremented or decremented according to the predetermined converged value of digital FIR filter 160." (Phanse, col. 10, lines 42-55, emphasis added)

"The above-described mixed mode equalization operation continues in subsequent process steps (such as exemplary process steps 630 and 635) until the coefficients of digital FIR filter 160 converge to the pre-determined threshold value, TH.sub.(AEF). At this point, no further adaptation of AEF 140 is required (process step 640) and the operation is complete." (Phanse, col. 11, lines 11-17, emphasis added)

The Applicant respectfully points out that PHANSE does not teach and disclose to perform only one of analog based compensation and digital based compensation, but in contradistinction, PHANSE teaches and discloses both analog based compensation and digital based compensation as being complementary and requisite in the proper operation thereof. The effective operation of PHANSE seems inextricably linked to this "mixed mode equalization" that employs both analog-based compensation and digital-based compensation.

As cited above, Phanse explicitly teaches and discloses that the "mixed mode equalization scheme provides some analog and some digital equalization to compensate for the overall attenuation of the channel". Clearly, Phanse clearly teaches and discloses that some of the equalization is "analog" and some of the equalization is "digital".

The Applicant respectfully believes that Phanse fails to teach and disclose subject matter that includes a digital signal processor that adaptively determines compensation operations to be performed by the receiver on the digital samples of the modulated serial data so that the digital samples of the modulated serial data may be properly characterized to extract digital data contained therein. The Applicant respectfully believes that Phanse likewise fails to teach and disclose each and every limitation of the subject matter as claimed by the Applicant in the Applicant's independent claim 1 and the Applicant's other independent claims.

Therefore, in light of at least these comments made above, the Applicant respectfully believes that Phanse fails to teach and disclose each and every limitation of

the subject matter as claimed by the Applicant in each of independent claims indicated above that the Examiner rejects as being anticipated by Phanse.

The Applicant also respectfully believes that the dependent claims indicated above that the Examiner rejects as being anticipated by Phanse, being further limitations of the subject matter as claimed in allowable independent claims are also allowable.

As such, in light of at least these comments made above, the Applicant respectfully requests that the Examiner withdraw the rejection of claims 1, 38, 42, 70-71, 80, 104, 113, 128, 134, 1714 under 35 U.S.C. § 102(b) as being anticipated by Phanse.

***Allowable Subject Matter***

7. In the office action, the Examiner states:

"Claims 129-133 are allowed." (office action, Part of Paper No./Mail Date 20061002, p. 4).

The Applicant respectfully believes that claims 1-184 are in condition for allowance and respectfully requests that they be passed to allowance.

The Examiner is invited to contact the undersigned by telephone or facsimile if the Examiner believes that such a communication would advance the prosecution of the present U.S. utility patent application.

RESPECTFULLY SUBMITTED,

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